33

**Sidewinder Development Board**

**rev 1.0**

|  |  |
| --- | --- |
| Features   * Altera MAX V CPLD 5M160ZT100C5 * JTAG programmable * USB programmable * USB powered * 12 On-board LEDs * 10 on-board switches * 3 RGB LEDs * One 40-pin expansion headers * One Dual multiplexed 7-segment display | http://www.dvhardware.net/news/2015/altera.jpg  Microchip Technology Inc  C:\Users\Alex\AppData\Local\Microsoft\Windows\INetCache\Content.Word\open_source_hardware_logo-t.png |

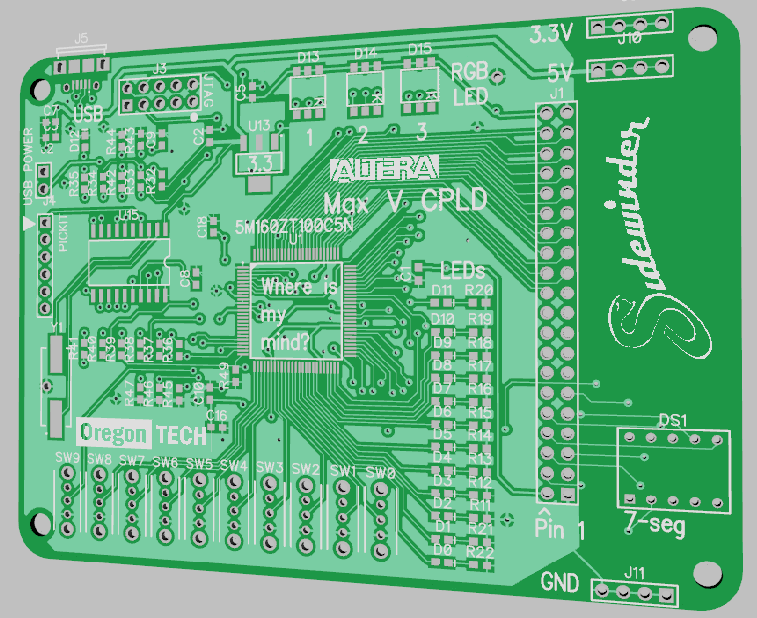


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# WARNING

Failure to read and adhere to the instructions in this manual may cause permanent and irreversible damage to your Sidewinder Board and computing equipment.

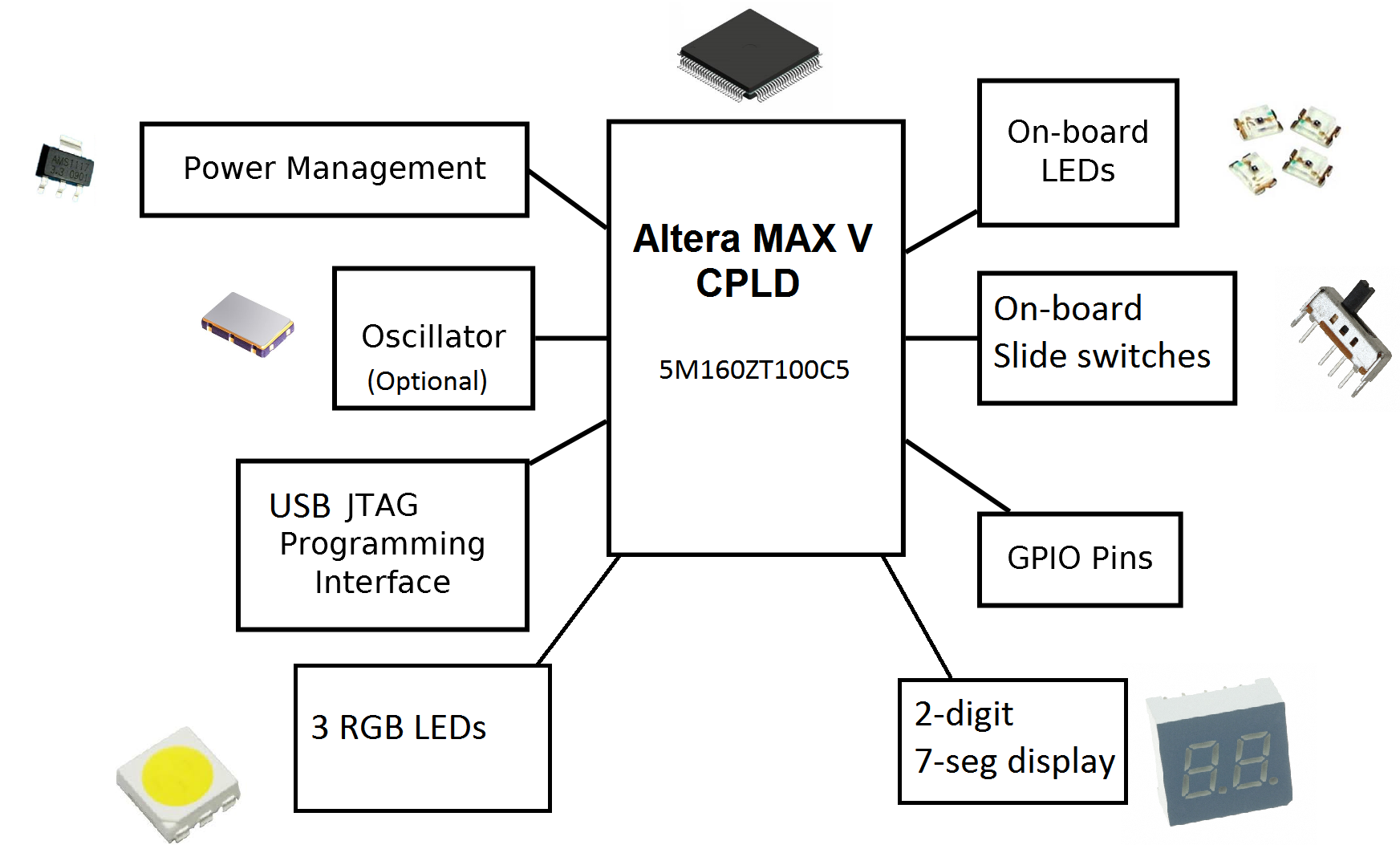
By using your Sidewinder board on your personal computer, you agree to hold Oregon Tech and affiliated parties entirely free from any liability, including financial responsibility for injuries incurred, regardless of whether injuries are caused by negligence.

Use at your own risk.

# 1.0 Hardware

This section describes the basic hardware features of the sidewinder board. For more specific part selections and PCB references, consult the BOM in the References section of this document.

## 1.1 Hardware Overview

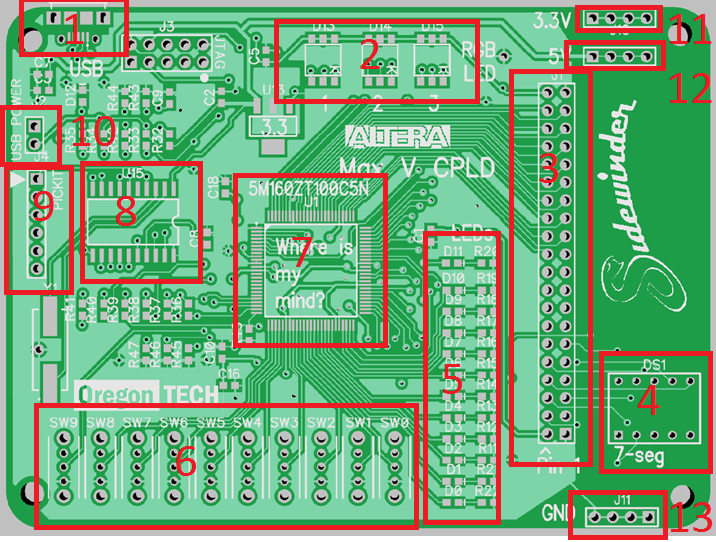


The Sidewinder board is a solid foundation to explore the fundamentals of digital logic, configurable hardware, and programmable logic devices. It provides the following features:

* Altera MAX V 5M160ZT100C5 in TQFP-100 package
* Three RGB LEDs
* Dual multiplexed 7-segment display
* 10 slider switches
* 12 LEDs
* 40-pin GPIO header
* Dual voltage rail: 3.3 V and 5 V

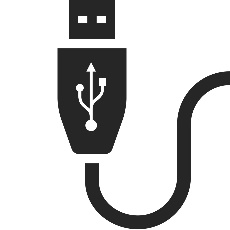
One 40-pin GPIO header on the board allow for direct connection to the FPGA’s logic pins. Headers on both sides of the prototyping area of the board offer 3.3 V, 5.0 V and GND busses. See appendix for pin mapping.

## 1.2 Board



|  |  |  |
| --- | --- | --- |
| # | Description |  |
| 1 | USB Micro |  |
| 2 | 3 RGB LEDs |  |
| 3 | 40-pin connector, 36 pin GPIO. |  |
| 4 | 7-segment multiplexed LED |  |
| 5 | 12 LEDs |  |
| 6 | 10 slide switches |  |
| 7 | 5M160ZT100C5N Max V CPLD |  |
| 8 | PIC USB Blaster emulation |  |
| 9 | PICKIT header |  |
| 10 | External power. | Jumper for USB. Pin towards switches for external power |
| 11 | 3.3 V header |  |
| 12 | 5.0 V header |  |
| 13 | GND header |  |

## 1.3 Additional hardware for USB compatibility

The USB programming circuitry is built into the Sidewinder board. It utilizes a PIC18F1450 processor to act as the USB Blaster. Connecting micro USB to the board should power the board. LED D12 should illuminate indicating that the board is on and ready to be programmed. The micro USB connection also serves as a programming interface.

## 1.4 Voltage WARNING

This board utilizes three voltages. 1.8, 3.3, and 5 V.

|  |  |  |
| --- | --- | --- |
| Name | Voltage | Purpose |
| VCCINT | 1.8 V | Power CPLD internal logic |
| VCCIO | 3.3 V | Power GPIO and all accessories on board |
| USB Input | 5 V | Power board |

When powering the board through the external header (J4), ensure 5 V is supplied to the board. Do not connect anything higher or lower than this voltage, as damage to board may occur. Note that the pin facing towards the switch is where you should apply 5 V. Ground can be connected to the ground bus on the board.

When powering through USB, assure that the device and connected accessories do not consume more than 400 mA on the 5 V rail.

# 2.0 Programming

## 2.1 Software Requirements

Whether using Windows or Linux, a valid copy of Quartus II v16 is required to synthesize HDL code into a binary file, readable by the FPGA. Consult Altera’s online resources to determine which version of Quartus II is compatible with the FPGA being used on the sidewinder board.

Do it at home!

You can work on this lab from home if you buy the Sidewinder development board and install Quartus II Lite on your PC. There is a free web edition of the Quartus II software available for download in case you wish to work with Quartus outside of lab. The download file is 1.8GB. You should also select ModelSim-Altera edition (1.4 GB), and MAX V device support.

## [*http://dl.altera.com/16.0/?edition=lite*](http://dl.altera.com/16.0/?edition=lite)

2.2 Hardware Setup

The following section outlines common hardware setup non-volatile programming mode. Please follow these wiring instructions carefully. Routing connections incorrectly can result in electrical shorts, rendering your Sidewinder board and/or computer inoperable.

WARNING: If powering sidewinder from external power source, remove USB power jumper and connect auxillury power to header.

 WARNING: Do not connect micro USB and external power source at the same time!

## 

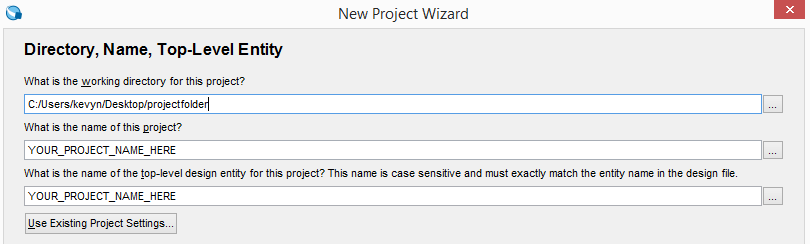
## 2.3 Setting up the project

### 2.3.1 Using the default template project

The default project template should be located on your course website. The default project template is an empty project pre-configured for the sidewinder board. It will have all GPIO pins, 7-segment displays, LEDs, RGB LEDs, mapped.

### 2.3.2 Creating the project file.

1. In the Quartus II main window, select FILE|NEW PROJECT WIZARD, and then click NEXT. The following window should launch.



1. Using the browse button in the top field, select the working directory you wish to use for the project.
2. Type inyour project nameas the Project Name. Click NEXT.
3. There are no files to add to this window, so click NEXT.
4. You will now select the CPLD device-type that will become the target for your Verilog HDL file design. See the screen capture below. Under Device family, select MAX V. Under Show In Available Device List, select TQFP for Package, pin count = 100. Select the 5M160ZT100C5. Click NEXT.

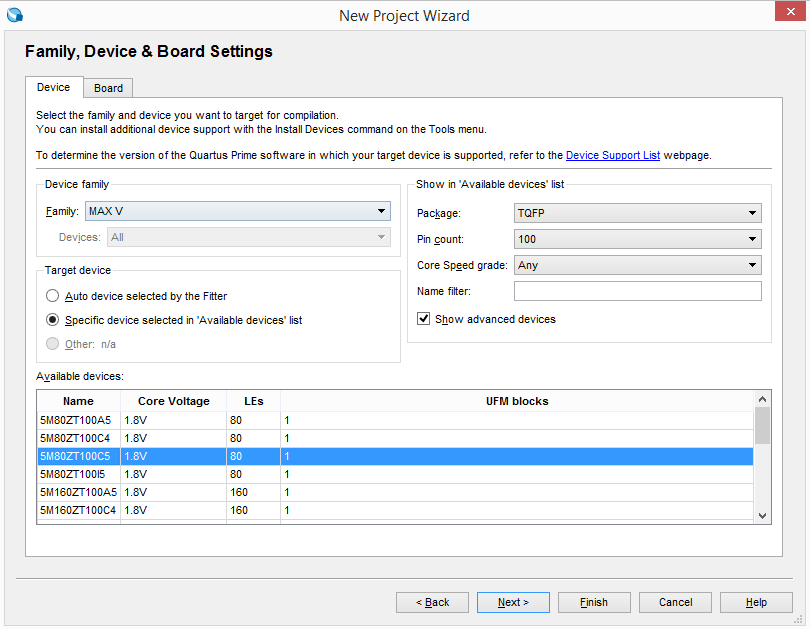
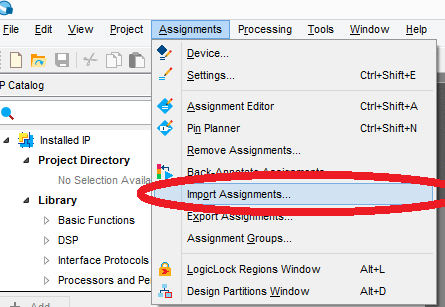
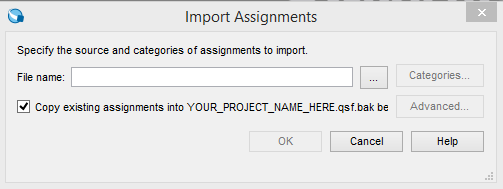
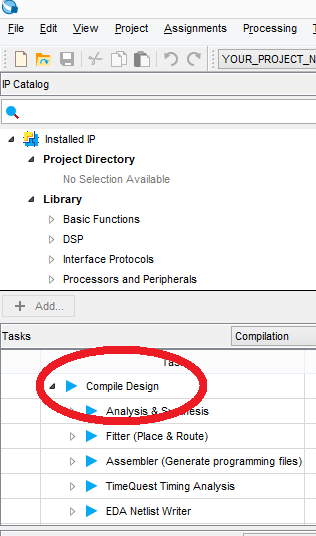


Figure 1

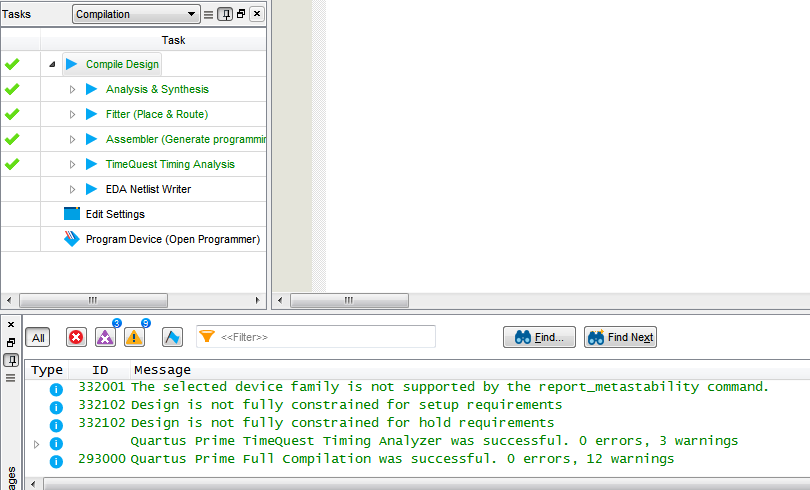
1. Since we are not using any third party tools, leave all lines as <None> and click NEXT.
2. You should see a summary page of the settings for your project. Click on FINISH.
3. Now, we will need to import the template qsf file. The QSF file is how Quartus maps your signal names to corresponding pins on the CPLD and Sidewinder development board.
4. Select ASSIGNMENTS| IMPORT ASSIGNMENTS.
5. Click on …
6. Navigate to your sidewinder QSF file. After selecting the sidewinder qsf file, click OK.

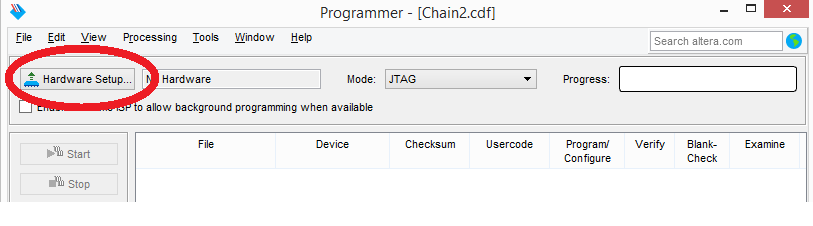
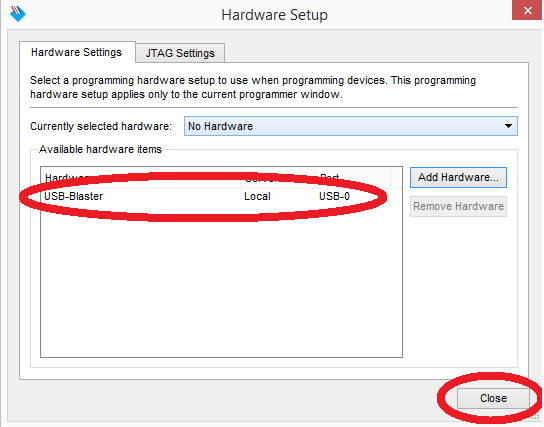
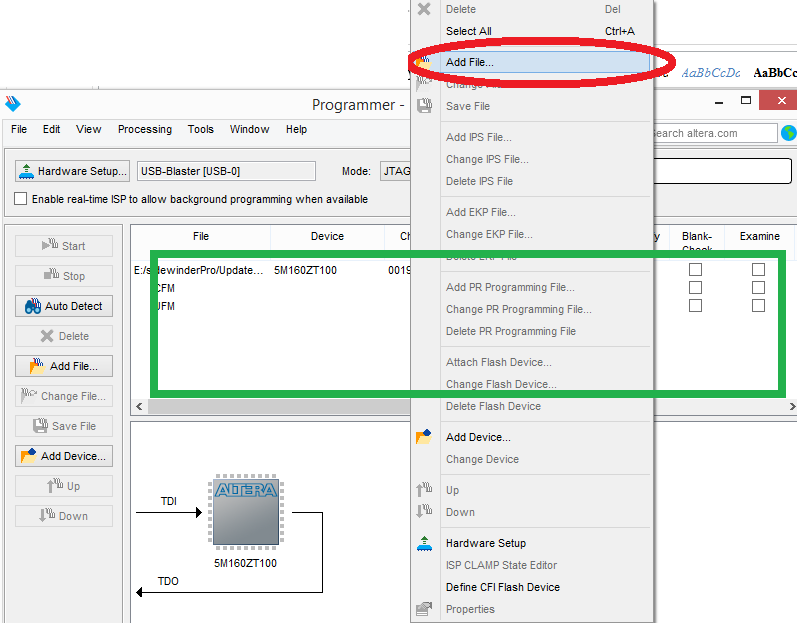
## 2.4 Programming



1. Make sure that you have successfully compiled the design.

You should see the following after successful compilation



1. Click TOOLS|PROGRAMMER, then the Hardware Setup button. 
2. Double click on USB-Blaster until it shows up as Currently selected hardware. Then click close. If you can’t see the USB-Blaster, make sure your Sidewinder board is plugged into the USB port. 
3. Also note, if you can not see the USB-Blaster, the driver may not be installed. Go to device manager and make sure that the device driver is installed. The location of the device driver is generally C:\Altera\{VERSION\_NUMBER}\quartus\drivers.
4. Right click anywhere inside the green box, and click on Add File. 
5. Navigate to your project on the student file server (the Z drive) and find the \*.pof, which is the Programming Object File from your project. Once you have located it, click Open. In the programmer window, you should now see your File name, the Device (5M160ZT100). There will be several checkboxes to the right of this information. Click the checkbox labeled Program/Configure. If there are any other devices, click on them and delete them, as they will cause your programming to fail.
6. Click on STARTin the left toolbar. Wait until the configuration of the CPLD successfully completes.

It is now configured and ready to test.

## 2.5 Troubleshooting

* Verify that your board is connected to the computer via micro USB.
* Power cycle the board
* Verify that your computer has the Altera USB Blaster device driver installed.
* Try another micro USB cable.
* Verify that your board’s D12 light is illuminated.

# 3.0 References

## 3.1 Supporting Documents

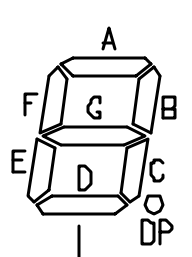
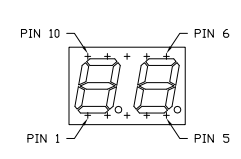
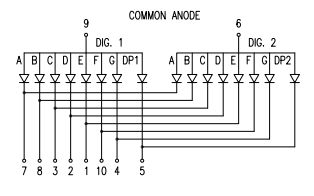
## 3.2 GPIO Pinout Descriptions

Looking at the board from the top (CPLD mounted), pin 1 is indicated by an arrow.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Header Pin # | Pin Description | GPIO in Quartus Software | Altera Max V TQFP 100 Pin # |  |
| 1 | 3.3 V |  | N/A |
| 2 | GND |  | N/A |
| 3 |  | IO[0] | 52 |
| 4 |  | IO[1] | 51 |
| 5 |  | IO[2] | 54 |
| 6 |  | IO[3] | 53 |
| 7 |  | IO[4] | 56 |
| 8 |  | IO[5] | 55 |
| 9 |  | IO[6] | 58 |
| 10 |  | IO[7] | 57 |
| 11 |  | IO[8] | 66 |
| 12 |  | IO[9] | 61 |
| 13 |  | IO[10] | 68 |
| 14 |  | IO[11] | 67 |
| 15 |  | IO[12] | 70 |
| 16 |  | IO[13] | 69 |
| 17 |  | IO[14] | 72 |
| 18 |  | IO[15] | 71 |
| 19 |  | IO[16] | 74 |
| 20 |  | IO[17] | 73 |
| 21 |  | IO[18] | 76 |
| 22 |  | IO[19] | 75 |
| 23 |  | IO[20] | 78 |
| 24 |  | IO[21] | 77 |
| 25 |  | IO[22] | 82 |
| 26 |  | IO[23] | 81 |
| 27 |  | IO[24] | 84 |
| 28 |  | IO[25] | 83 |
| 29 |  | IO[26] | 86 |
| 30 |  | IO[27] | 85 |
| 31 |  | IO[28] | 88 |
| 32 |  | IO[29] | 87 |
| 33 |  | IO[30] | 90 |
| 34 |  | IO[31] | 89 |
| 35 |  | IO[32] | 92 |
| 36 |  | IO[33] | 91 |
| 37 |  | IO[34] | 96 |
| 38 |  | IO[35] | 95 |
| 39 | 3.3 V |  | N/A |
| 40 | GND |  | N/A |

## 3.3 7-segment Pinout Descriptions

The 7-segment is a multiplexed model sharing pins with GPIO. Model number LDD-E2802RD or similar.



[http://www.lumex.com/content/files/ProductAttachment/LDD-E2802RD.pdf]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 7-seg Pin # | Header Pin # | Signal Name | FPGA Pin # | Segment |
| 1 | 4 | SEG[5] | 62 | E |
| 2 | 3 | SEG [4] | 61 | D |
| 3 | 6 | SEG [3] | 58 | C |
| 4 | 5 | SEG [7] | 55 | G |
| 5 | 8 | SEG [0] | 54 | DP1 |
| 6 | 7 | SEGA[0] | 51 | DIGIT2 ANODE |
| 7 | 10 | SEG [1] | 57 | A |
| 8 | 9 | SEG [2] | 53 | B |
| 9 | 12 | SEGA[1] | 56 | DIGIT1 ANODE |
| 10 | N/A | SEG [6] | 52 | F |

## 3.4 LED Pinout Descriptions

**3.4.1 RGB LEDs**

When using the default template file, Pin Planner in Quartus configures pins as output 3.3 V LVCMOS.

The RGB LEDs are active low. Setting pin to logic ‘0’ will turn on LED.

|  |  |  |
| --- | --- | --- |
| Name in Quartus | Pin Location on MAX V | Color |
| RGB1[0] | 3 | R |
| RGB1[1] | 4 | G |
| RGB1[2] | 2 | B |
| RGB2[0] | 98 | R |
| RGB2[1] | 99 | G |
| RGB2[2] | 97 | B |
| RGB3[0] | 6 | R |
| RGB3[1] | 7 | G |
| RGB3[2] | 5 | B |

**3.4.2 LEDs**

When using the default template file, Pin Planner in Quartus configures pins as output 3.3 V LVCMOS.

The LEDs are active high. Setting pin to logic ‘1’ will turn on LED.

|  |  |
| --- | --- |
| Name in Quartus | Pin Location on MAX V |
| D[0] | 37 |
| D[1] | 38 |
| D[2] | 39 |
| D[3] | 40 |
| D[4] | 41 |
| D[5] | 42 |
| D[6] | 43 |
| D[7] | 44 |
| D[8] | 47 |
| D[9] | 48 |
| D[10] | 49 |
| D[11] | 50 |

## 

## 3.5 Switch Pinout Descriptions

When using the default template file, the Pin Planner in Quartus sets the switch pins as input 3.3V LVCMOS with weak pull-up enable resistors enabled. If creating your own project, you will need to configure the Max V internal weak pull-up enable resistors.

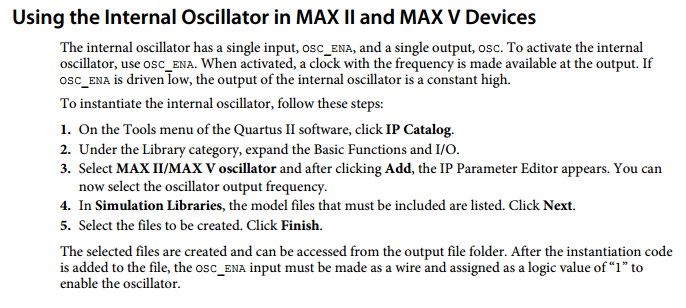
|  |  |
| --- | --- |
| Name in Quartus | Pin Location on MAX V |
| SW[0] | 36 |
| SW[1] | 35 |
| SW [2] | 34 |
| SW [3] | 33 |
| SW [4] | 30 |
| SW [5] | 29 |
| SW [6] | 28 |
| SW [7] | 27 |
| SW [8] | 26 |
| SW [9] | 21 |

## 3.1 Crystal Oscillator

### 3.1.1 Internal Oscillator

The base Sidewinder operates on a variable internal oscillator. The MAX V frequency range is 15.60 to 21.20 MHz. The maximum possible output of the internal oscillator to an external pin is 3.9-5.3 MHz.

When using the internal oscillator, remember to enable the internal oscillator in your pin planner.

[Altera App Note AN496]

See the Altera Application Note AN496 for more information.

<https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an496.pdf>

3.1.2 External oscillator

The external oscillator is not populated by default to reduce board cost. The Sidewinder is designed to hold a Fox Electronics FXO-HC735 family oscillator in slot CRY1. You can install an oscillator if desired. The oscillator is wired to PIN 12, CLK0.

## 3.2 Bill of Materials (BOM)

The BOM is subject to change due to continuous improvement.

DNP = Do not populate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| # | RefDes | Footprint | Description | Part Number | Quantity |
| 1 | C1, C4, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18 | CAP\_0603 | Generic | 0.1 uF | 13 |
| 2 | C2, C3 | CAP\_0603 | Generic | 100 nF | 2 |
| 3 | C5, C6 | CAP\_0603 | Generic | 10 uF | 2 |
| 4 | C7 | CAP\_0603 | Generic | 1 uF | 1 |
| 5 | D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12 | 0603 LEDs | Generic | 0603 BLUE LED | 13 |
| 6 | D13, D14, D15 | 5050 RGB LED | Generic | 5050 RGB LED | 3 |
| 7 | DS1 | 7-segment display 2 digit | Lumex | 696-LDD-E2802RD | 1 |
| 8 | GS1, GS2, GS3 | Short |  |  | DNP |
| 9 | J1 | 0.1" 20x2 header | Generic | Male 20x2 0.1" header | 1 |
| 10 | J2 | 0.1" 1x2 header | Generic | Male 2x1 0.1" header | 1 |
| 10 | J3 | 0.1" 2x5 header | Generic | Male 2x5 0.1" header | DNP |
| 11 | J4 | 0.1" 6x1 header | Generic | No populate | DNP |
| 12 | J5 | USB |  | ZX62D-B-5PA8 | 1 |
| 13 | J9, J10, J11 | 0.1" 4x1 headers | Generic | Male 4x1 0.1" header | 3 |
| 14 | R1, R2, R3, R4, R5, R6, R7, R8, R9, R35 | RES\_0603 | Generic | 330 Ohm | 6 |
| 15 | R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22 | RES\_0603 | Generic | 1K Ohm | 12 |
| 16 | R32 | RES\_0603 | Generic | 10K Ohm | 1 |
| 17 | R33, R34, R36, R37, R38, R39, R40, R41, R42 | RES\_0603 | Generic | 100 Ohm | 9 |
| 18 | R43, R44, R45, R46, R47, R49 | RES\_0603 | Generic | 200 Ohm | 6 |
| 19 | R51, R52, R53, R54, R55, R56, R57 | RES\_0603 | Generic | 330 Ohm | 7 |
| 20 | SW0, SW1, SW2, SW3, SW4, SW5, SW6, SW7, SW8, SW9 | Through-hole | SPDT switch COMAX | SS-12D07-VG 4 NS GA PA | 10 |
| 21 | U1 | CPLD | Altera | 5M160ZT100C5N | 1 |
| 22 | U13 | 3.3V regulator | AMS | AMS1117-3.3 | 1 |
| 23 | U14 | 1.8V regulator | AMS | AMS1117-1.8 | 1 |
| 24 | U15 | Pic 18f14k50 SOIC 20 | MICROCHIP | PIC18F14K50-I/SO-ND | 1 |
| 25 | Y1 | 12 MHZ Crystal | Generic | ABLS-12.000MHZ-B4-T | 1 |
| 26 | CRY1 | 24 MHZ Oscillator | Fox Semiconductor | FOX FXO-HC735-25 | DNP |
| 27 | FUSE1 | USB protection | Bel Fuse | 0ZCG0050AF2C | 1 |
| 28 | C19, C20 | CAP\_0603 | Generic | 15 pF | DNP |
|  |  |  |  |  |  |

## 3.3 Schematics

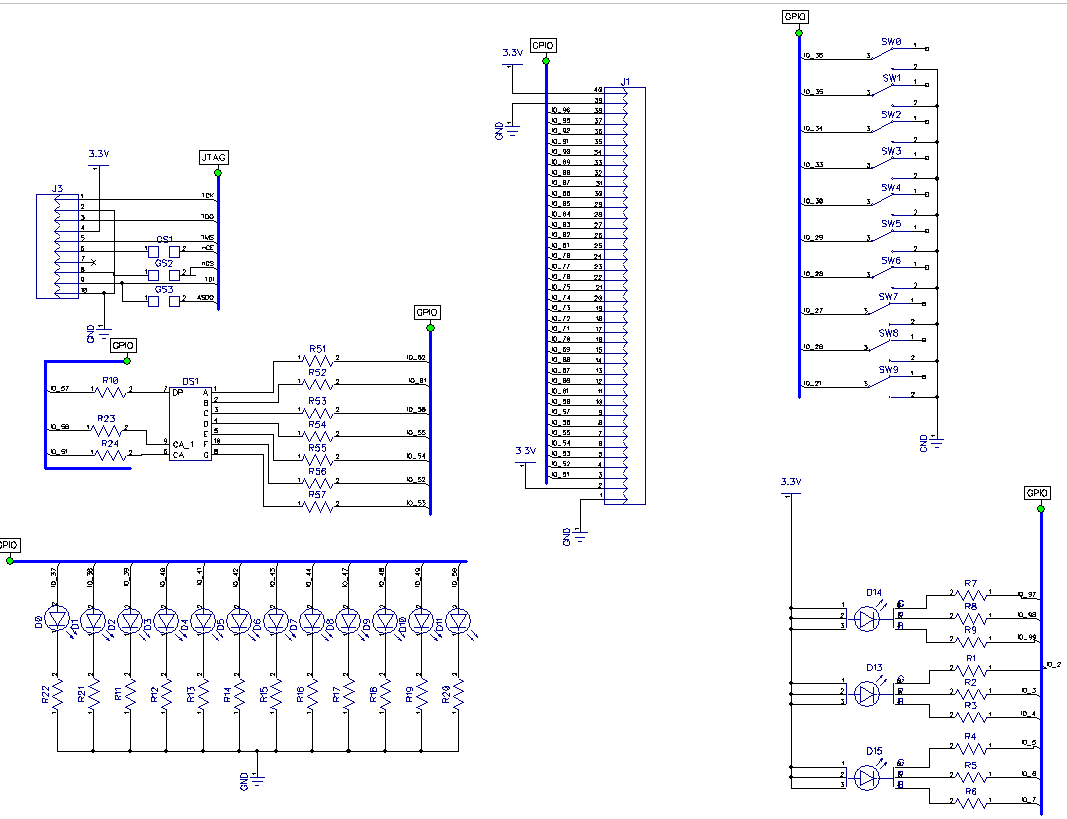
## 

USB Blaster Circuit

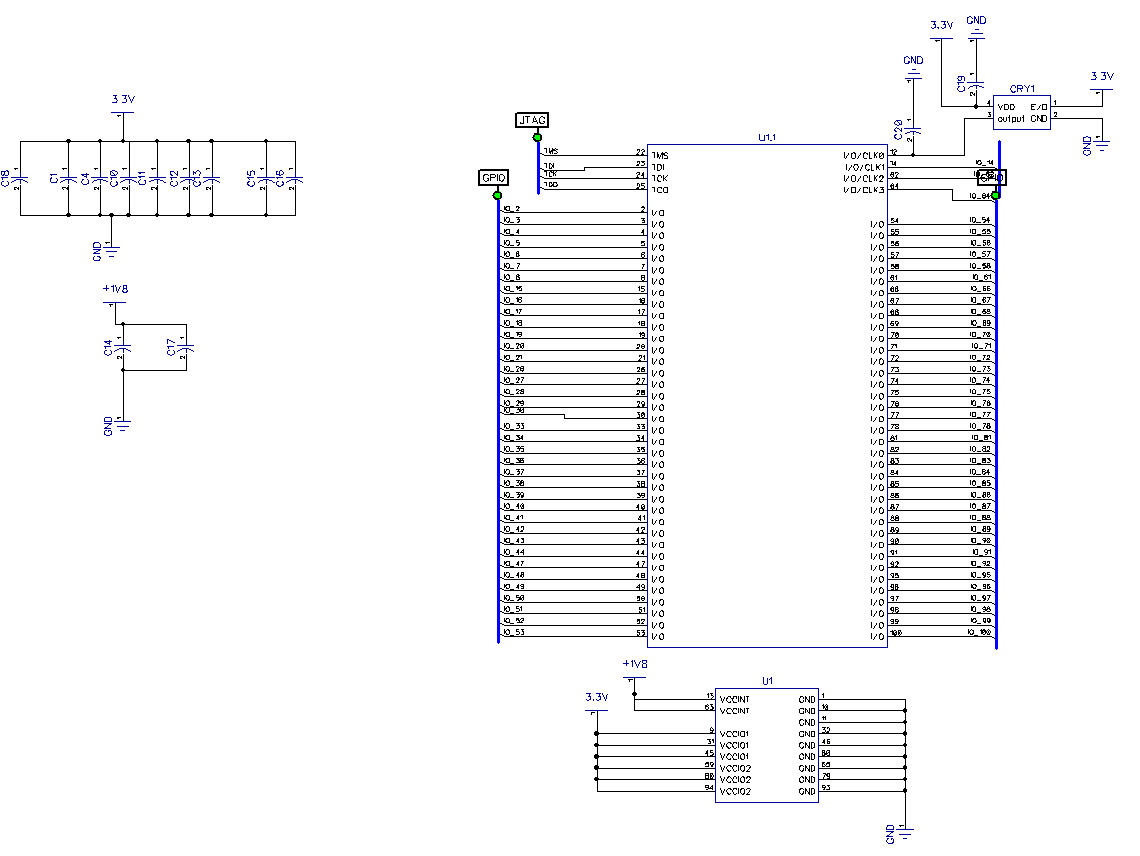
Using firmware and schematic from: http://www.sa89a.net/mp.cgi/ele/ub.htm

## 

Power System



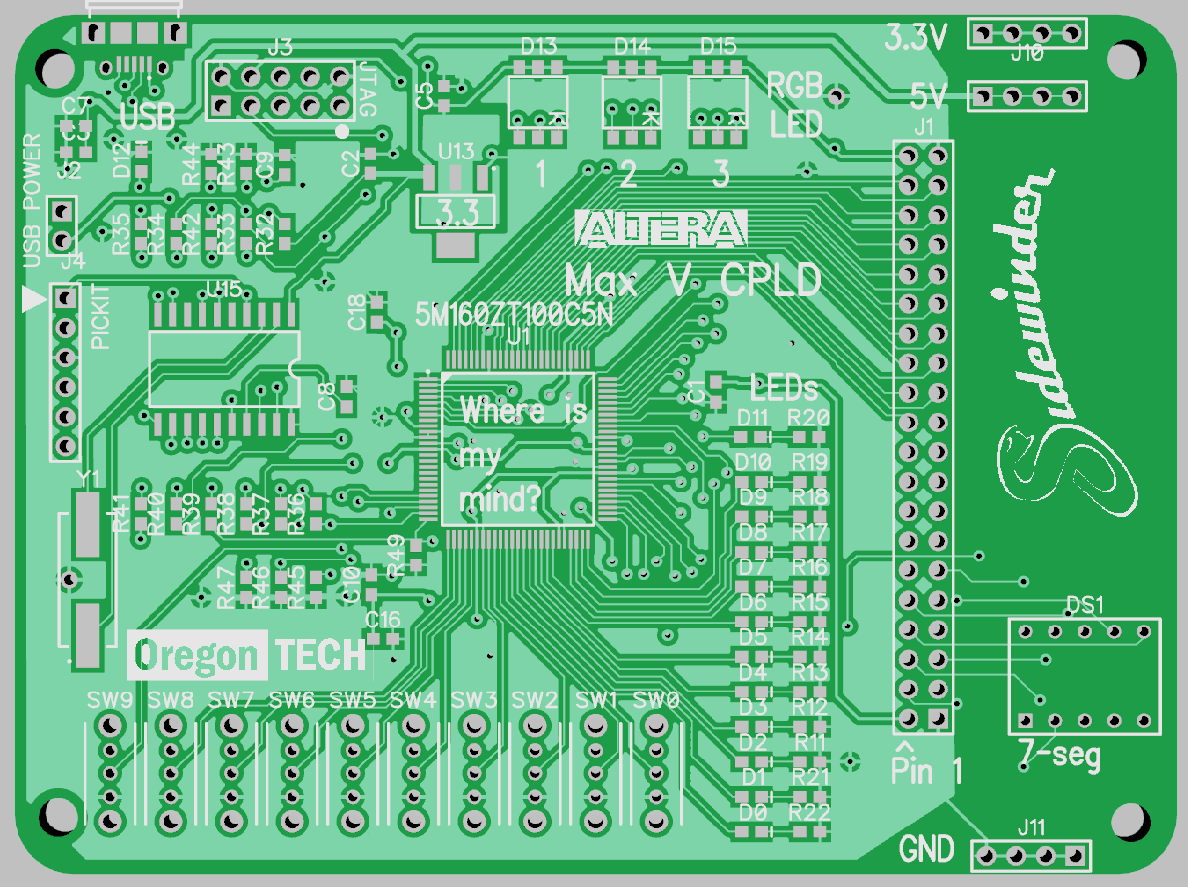
I/O: JTAG, 7-segment, GPIO, LEDs, and RGB LEDs

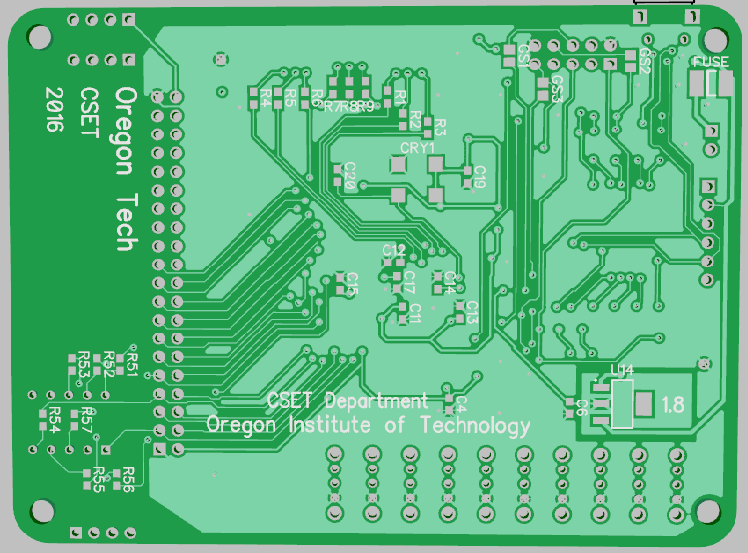


MAX V CPLD 5M160ZT100C5N

## 3.4 PCB Layout

Front



Back

# 4.0 Document History

|  |  |  |
| --- | --- | --- |
| Document Revision | Date | Author |
| v. 0.1 - Initial write-up (Conversion from OwlBoard) | June 1, 2015 | Alexander Hogen |
| v. 0.2 – Update document for jumperBoard | July 25, 2016 | Kevin Pintong |
| v. 0.3 – Add Errata, Fix 7-segment | August 3, 2016 | Kevin Pintong |
| v. 0.4 – Fix 7-segment for easier mapping | September 12, 2016 | Kevin Pintong |
| V 0.5 – Fix RGB LED mapping | October 31, 2016 | Kevin Pintong |

# 5.0 Important Notes

|  |  |  |
| --- | --- | --- |
| Board Revision | Date | Author |
| Initial Design for Max 10 | June 1, 2015 | Dustin Henderson |
| v1- Downgrade to Max V, Altera chips delayed | July 25, 2016 | Kevin Pintong |
| v2- Wrong 7-segment routing | August 3, 2016 | Kevin Pintong |
| v3- Corrected 7-segment, 40 pin moved | September 12, 2016 | Kevin Pintong |

# 5.1 Errata

As of September 12, 2016, you have a v3 board.

Board v1 (Initial design version)

* 7-segment is routed incorrectly.
  + Resolution: Do not use.
* No jumper for removal of USB power. Board can only be powered via USB.
  + Resolution: Do not plug in other power sources.
* VUSB pin is tied to 5V instead of GND.
  + Resolution: Lift pin 17 on U15, solder 1 uF capacitor and route to GND node.

Board v2(Faculty Sample version)

* 7-segment is routed incorrectly. Do not use.

Board v3 (Production / Student version)

* None found so far (8/3/16)
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